ALPHA DATA

# FMC-IO68
# User Manual

**Document Revision: 1.2**
**14th October 2015**

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# 1 Introduction

The FMC-IO68 is a VITA 57.1 compliant single width HPC FMC module, designed for use with Alpha Data's VITA 57.1 compliant carrier cards. It provides the user with 68 IO signals to an industry standard SCSI connector.

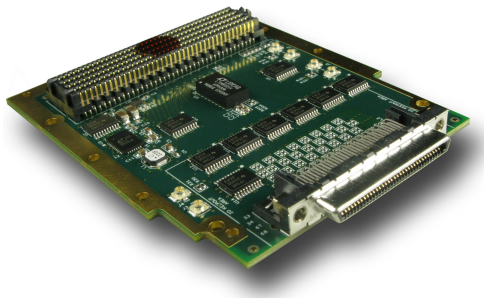

**Figure 1 : FMC-IO68 Image**

**Key Features**

- FMC (VITA 57.1) compliant
- Conduction and air cooled compatible
- 68 single ended (34 differential) signals routed to VHDCI 68 position SCSI
- Operating temperature range from -45 to 85 degrees Celsius
- Level shifting and resistor fit options for application customization
- Up to 4x serial channels and 4x 3.3V GPIO on Alpha Data FMC GPIO

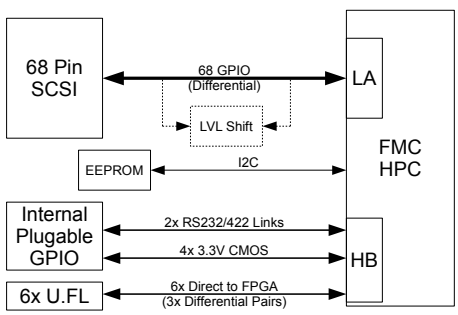


**Figure 2 : FMC-IO68 Block Diagram**

## 1.1 References & Specifications

| | |
|---|---|
| ANSI/VITA 57.1 | FPGA Mezzanine Card (FMC) Standard, February 2010, VITA, ISBN 1-885731-49-3 |

**Table 1 : References**

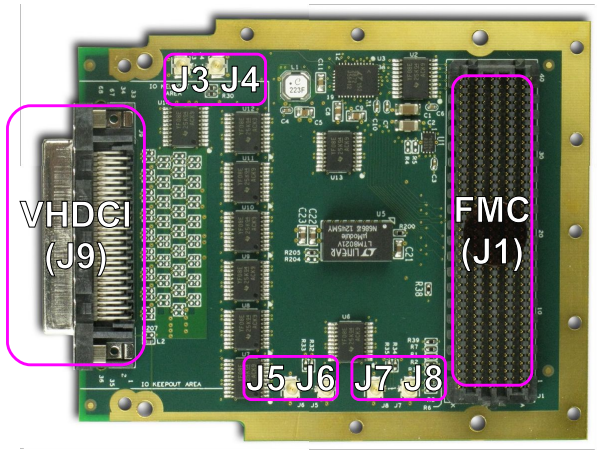


**Figure 3 : FMC-IO68 Top Side Features**

# 2 User Input/Output Signals

## 2.1 Level Shifting Options

**Level Shifting Options**

The 68 signals from the FMC connector have three Level shifting options:

1. Direct Connect: This option fits resistor that tie the VHDCI pins directly to the FMC pins. This option supports both differential signaling standards (i.e. LVDS) and single ended (i.e. CMOS) directly to an FPGA. However the maximum supported IO voltage of the FPGA must be considered when using this option.
2. 3V3: This option fits auto-direction sensing level shifters that are push-pull and open-drain compatible between the FMC and VHDCI connector. The IO level of the level shifters is 3.3V CMOS compatible. These level shifters do not support differential signaling. The FPGA IO bank can operate down to 1.2V with this option.
3. 5V0: This option fits auto-direction sensing level shifters that are push-pull and open-drain compatible between the FMC and VHDCI connector. The IO level of the level shifters is 5.0V CMOS compatible. These level shifters do not support differential signaling. The FPGA IO bank can operate down to 1.2V with this option.

**Note:**
When using the level translators, be sure to carefully read the application note describing the operation of the circuit found here: http://www.ti.com/lit/an/scea044/scea044.pdf
Note in particular the points about load capacitance and wire length.

**Note:**
The level shifters are 8 bits wide and can be fitted in a custom configuration to allow some direct connect and some buffered signals through the same VHDCI connector. Contact sales@alpha-data.com for more details.

## 2.2 Ground Connections

Each signal has a resistor site that can be fitted to tie the signal directly to ground. This can be used to enhance signal integrity and provide a ground reference in the cable. Contact sales@alpha-data.com for more details.

By default the case of the VHDCI connector is tied to Chassis Ground. The case can be tied to signal ground instead, contact sales@alpha-data.com for more details.

## 2.3 VHDCI SCSI Connector

**Receptacle**
The VHDCI SCSI connector on the FMC-IO68 is a widely used industry standard connector that provides screw lock retention. The part is available from multiple manufactures.

- Ultra+ VHDCI connector system: Molex part number 71430-0008

**Figure 4 : VHDCI Cable**

# 3 General Purpose IO

## 3.1 Overview

This FMC module provides the user access to a number of general purpose connectors that can be used for many different functions. The GPIO interface can be broken down into three components:

### 3.1.1 Direct Connections to the FPGA

There are three differential pairs accessible through industry standard U.FL connectors. These pairs are ideal for clocking and synchronization.

### 3.1.2 Serial Interface

**Serial Transceiver Configurations**
The FMC hosts a Linear Technology LTC2872 configurable serial transceiver. This transceiver can be configured through strapping resistors to run in the following configurations:

- 4 channels of RS232
- 2 channels of RS232 and 1 channel of RS422
- 2 channels of 422

The default mode of operation is: 2 channels of 422. Please see the LTC2872 datasheet for more details on configurability. All 11 configuration signals are tied to strapping resistors and can be configured to your specific needs by contacting sales@alpha-data.com.

### 3.1.3 General Purpose IO

Four signals from the FPGA are level translated to 3.3V and made available on the GPIO connector. The level translator is capable of driving both open-drain and push-pull signals.

## 3.2 Connectors

**Receptacles**
In order to guarantee the safety of the FPGA and enhance usability, this GPIO interface has been broken into multiple connectors.

- GPIO Connector: I-PEX part number 20455-020E-12
- UFL Connector: Hirose part number U.FL-R-SMT-1(10)

## 3.3 Mating Cables

**Receptacles**
Below is a list of possible mating cables for each associated receptacle.

- GPIO Connector: Alpha Data adapter pigtail part number AD-FMC-GPIO
- UFL Connector: Industry standard U.FL cable (multiple vendors)

# 4 Installation

The FMC-IO68 is designed to plug into the FMC front panel connector on a compatible carrier. The retaining screws should be tightened to secure the FMC.

**Note:**
This operation should not be performed while the host carrier is powered.

## 4.1 Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions and avoid flexing the board.

## 4.2 IO Voltage Selection

The required IO voltage range (VADJ) for the FMC is 1.2V to 3.3V. This is stored in a ROM on the FMC, as per VITA 57.1 for automatic configuration of supplies. The carrier is responsible for detecting and setting the IO voltage accordingly.

# 5 Order Code

| Product Code | FMC-IO68 (v) |
|---|---|
| IO Voltage (v) | Blank = Direct Connect to FPGA<br>/3V3 = 3.3V Bidirectional Buffer<br>/5V0 = 5.0V Bidirectional Buffer |

**Table 2 : Order Code**

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# Appendix A: VHDCI Pin Assignments

| Signal | FMC (J1) | VHDCI (J9) | | VHDCI (J9) | FMC (J1) | Signal |
|---|---|---|---|---|---|---|
| LA00_CC_P | G6 | 1 | \| | 35 | G7 | LA00_CC_N |
| LA01_CC_P | D8 | 2 | \| | 36 | D9 | LA01_CC_N |
| LA02_P | H7 | 3 | \| | 37 | H8 | LA02_N |
| LA03_P | G9 | 4 | \| | 38 | G10 | LA03_N |
| LA04_P | H10 | 5 | \| | 39 | H11 | LA04_N |
| LA05_P | D11 | 6 | \| | 40 | D12 | LA05_N |
| LA06_P | C10 | 7 | \| | 41 | C11 | LA06_N |
| LA07_P | H13 | 8 | \| | 42 | H14 | LA07_N |
| LA08_P | G12 | 9 | \| | 43 | G13 | LA08_N |
| LA09_P | D14 | 10 | \| | 44 | D15 | LA09_N |
| LA10_P | C14 | 11 | \| | 45 | C15 | LA10_N |
| LA11_P | H16 | 12 | \| | 46 | H17 | LA11_N |
| LA12_P | G15 | 13 | \| | 47 | G16 | LA12_N |
| LA13_P | D17 | 14 | \| | 48 | D18 | LA13_N |
| LA14_P | C18 | 15 | \| | 49 | C19 | LA14_N |
| LA15_P | H19 | 16 | \| | 50 | H20 | LA15_N |
| LA16_P | G18 | 17 | \| | 51 | G19 | LA16_N |
| LA17_CC_P | D20 | 18 | \| | 52 | D21 | LA17_CC_N |
| LA18_CC_P | C22 | 19 | \| | 53 | C23 | LA18_CC_N |
| LA19_P | H22 | 20 | \| | 54 | H23 | LA19_N |
| LA20_P | G21 | 21 | \| | 55 | G22 | LA20_N |
| LA21_P | H25 | 22 | \| | 56 | H26 | LA21_N |
| LA22_P | G24 | 23 | \| | 57 | G25 | LA22_N |
| LA23_P | D23 | 24 | \| | 58 | D24 | LA23_N |
| LA24_P | H28 | 25 | \| | 59 | H29 | LA24_N |
| LA25_P | G27 | 26 | \| | 60 | G28 | LA25_N |
| LA26_P | D26 | 27 | \| | 61 | D27 | LA26_N |
| LA27_P | C26 | 28 | \| | 62 | C27 | LA27_N |
| LA28_P | H31 | 29 | \| | 63 | H32 | LA28_N |
| LA29_P | G30 | 30 | \| | 64 | G31 | LA29_N |
| LA30_P | H34 | 31 | \| | 65 | H35 | LA30_N |
| LA31_P | G33 | 32 | \| | 66 | G34 | LA31_N |
| LA32_P | H37 | 33 | \| | 67 | H38 | LA32_N |
| LA33_P | G36 | 34 | \| | 68 | G37 | LA33_N |

**Table 3 : VHDCI Pin Assignments**

# Appendix B: Alpha Data GPIO Pin Assignments

| FMC Signal | FMC (J1) | Function (Connector) | | Function (Connector) | FMC (J1) | FMC Signal |
|---|---|---|---|---|---|---|
| HB00_CC_P | K25 | UFL_0_P (J3) | \| | UFL_0_N (J4) | K26 | HB00CC__N |
| HB01_P | J24 | UFL_1_P (J5) | \| | UFL_1_N (J6) | J25 | HB01_N |
| HB02_P | F22 | UFL_2_P (J7) | \| | UFL_2_N (J8) | F23 | HB02_N |
| HB03_P | E21 | DY1 (Serial TX) | \| | RA1 (Serial RX) | E22 | HB03_N |
| HB04_P | F25 | DY2 (Serial TX) | \| | RA2 (Serial RX) | F26 | HB04_N |
| HB05_P | E24 | GPIO_0 | \| | GPIO_1 | E25 | HB05_N |
| HB06_CC_P | K28 | - | \| | - | K29 | HB06_CC_N |
| HB07_P | J27 | GPIO_2 | \| | GPIO_3 | J28 | HB07_N |

**Table 4 : GPIO Locations**

# Revision History

| Date | Revision | Changed By | Nature of Change |
|---|---|---|---|
| 12 Nov 2013 | 1.0 | K. Roth | Initial Release |
| 20 May 2014 | 1.1 | L. Allison | Added VHDCI Columns to Appendix Appendix A |
| 14 Oct 2015 | 1.2 | K. Roth | Added note in Level Shifting Options pointing to the level translator application note. |

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